Independent Claims

1. A microcontroller for industrial control comprising:

    a central processing unit (CPU);

    a bus interface in communication with the CPU;

    a CPU memory module in communication with the bus interface; the CPU memory module configured to include a FIFO memory buffer;

    a direct memory access module in communication with the bus interface; and

    a serial peripheral interface (SPI) module in communication with the direct memory access module and the bus interface; the SPI module having hardware configured to maintain pointers to addresses within the FIFO memory buffer; the SPI module hardware configured to maintain counters; and the SPI module configured to use the FIFO memory buffer, pointers and counters as a transmission buffer for external communications for creating a virtual special function register.

2. The microcontroller of claim 1 the SPI module further comprising a transmitter buffer and a receiver buffer; wherein the transmitter buffer is configured to transmit data from the FIFO memory buffer, and wherein the receiver buffer is configured to transmit data to the FIFO memory buffer.

3. The microcontroller of claim 1 the SPI module further configured to operate as one of a master device and a slave device.

4. The microcontroller of claim 1 the SPI module further configured to provide a data register chip select signal.

5. The microcontroller of claim 1 the SPI module further configured to provide at least one of a CPU transmitter pointer signal, a CPU receiver pointer signal, a SPI transmitter pointer signal and a SPI receiver pointer signal.

6. The microcontroller of claim 1 the microcontroller further comprising a DMA module configured to communicate with the SPI module and the bus interface for providing cycle stealing.

7. A serial peripheral interface (SPI) for use with a microcontroller and configured for increasing the rate of data communications, wherein the SPI module comprises:

a plurality of hardware pointers to memory locations in a FIFO buffer;

at least one hardware pointer counter; and

a hardware logic device; wherein the hardware logic device is configured to communicate with a bus interface and to utilize the FIFO buffer for intermediate storage of data being transmitted from and received to the CPU.

8. The SPI of claim 7 wherein the plurality of hardware pointers are configured to provide at least one of a CPU transmitter pointer signal, a CPU receiver pointer signal, a SPI transmitter pointer signal and a SPI receiver pointer signal.

9. The SPI of claim 7 the SPI module further comprising a transmitter buffer and a receiver buffer; wherein the transmitter buffer is configured to transmit data from the FIFO buffer, and wherein the receiver buffer is configured to transmit data to the FIFO buffer.

10. The SPI of claim 7 the SPI module further configured to operate as one of a master device and a slave device.

11. The SPI of claim 7 the SPI module further configured to provide a data register chip select signal to the bus interface.

12. The SPI of claim 7 the SPI further configured to communicate with a DMA module and the bus interface for providing cycle stealing.

13. A method for increasing a microprocessor data communication rate through a serial peripheral interface (SPI) module comprising the steps of:

a) storing a first value from a Central Processing Unit (CPU) to a virtual special function register (SFR);

b) retrieving the first value from the virtual SFR and transmitting the first value through a Serial Peripheral Interface (SPI) module;

c) receiving a second signal at the SPI module and storing the second signal in the virtual SFR; and

d) communicating the second signal from the virtual SFR to the CPU;

wherein the virtual SFR comprises memory addresses within a circular FIFO buffer; and wherein the memory addresses within the circular FIFO buffer are identified by hardware pointers in the SPI module.

14. The method of claim 13 further comprising the step of using cycle stealing techniques; wherein a DMA module is configured to communicate with the bus interface and SPI module.

15. The method of claim 14 wherein the step of storing the first value further comprises the steps of:

providing a write signal, a virtual SFR address signal, and a data signal from the CPU to the SPI module;

sending, to a bus interface from the SPI module, a DRCS signal, and a CPU transmitter pointer address signal; and

writing from the bus interface to a FIFO memory device at an address indicated by the transmitter pointer address signal.

16. The method of claim 14 wherein the step of retrieving the first value further comprises the steps of:

detecting the presence of data to be sent on the FIFO buffer;

sending a SPI transfer request signal and a SPI transfer pointer signal to a DMA module;

requesting, by the DMA module, bus interface time and providing a DMA address signal and a DMA read signal to the bus interface;

reading a first value from the DMA address in the FIFO memory buffer to the bus interface;

providing the first value from the bus interface to the DMA module, and providing the first value from the DMA module to the SPI module; and

transmitting the data via a transmit shift register and transmit buffer.

17. The method of claim 16 wherein the step of retrieving the first value further comprises the steps of:

receiving an acknowledgement from the bus interface at the DMA module indicating

that the FIFO memory has been read; and

providing the acknowledgement to the serial peripheral interface module.

18. The method of claim 14 wherein the step of receiving and storing the second value further comprises the steps of:

sending the second value received at the SPI module to a DMA module;

sending a SPI receive request signal and a SPI receive pointer signal to a DMA module;

sending a DMA request signal, DMA write signal, DMA address signal and DMA data signal to the Bus interface; and

writing the DMA data signal to the FIFO buffer, and keeping track of the storage location by use of pointers in the serial peripheral interface;

19. The method of claim 14 wherein the step of receiving and storing the second value further comprises the steps of:

receiving an acknowledgement at the DMA indicating the second value was written to the FIFO buffer; and

sending the acknowledgement from the DMA module to the SPI module.

20. The method of claim 14 wherein the step of communicating the second value further comprises the steps of:

receiving, at a bus interface and SPI module, a read command signal and virtual SFR address signal from the CPU;

sending a data register chip select signal and FIFO pointer address to the bus interface; wherein the FIFO memory address is the address indicated by a pointer stored in the SPI module; and

reading the second value from that memory location to the CPU.